IN THE CLAIMS:

1. (currently amended) A built-in self-test controller ~~including~~ comprising[[:]] a memory built-in self-test engine ~~capable of executing~~ configured to execute a memory built-in self-test[[;]] and to generate a memory built-in self-test signature ~~generated~~ on execution of the memory built-in self-test wherein the built-in self-test signature comprises memory built-in self-test engine states.

2. (currently amended) The built-in self-test controller of claim 1, wherein the memory built-in self-test signature ~~register includes~~ comprises the results of at least one paranoid check.

3. (currently amended) The built-in self-test controller of claim 1, wherein the memory built-in self-test signature ~~includes~~ comprises a bit indicating whether the memory built-in self-test is done.

4. (currently amended) The built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine ~~operating~~ configured to operate the memory built-in self-test state machine.

5. (currently amended) The built-in self-test controller of claim 4, wherein the memory built-in self-test state machine ~~comprises~~ is configured to assume:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in ~~the~~ a memory built-in self-test domain in the initiate state;

a test state entered into from the flush state upon completing a flush of a plurality of memory components to a known state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

6. (currently amended) The built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine ~~operating~~ configured to operate a predetermined one of the memory built-in self-test state machines.

7. (currently amended) The built-in self-test controller of claim 6, wherein each of the memory built-in self-test ~~engines comprises~~ state machines is configured to assume:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state; and

a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

8. (currently amended) The built-in self-test controller of claim 1, further comprising:

a logic built-in self-test engine ~~capable of executing~~ configured to execute a logic built-in self-test and storing the results thereof; and

a multiple input signature register ~~capable of storing~~ configured to store the results of an executed logic built-in self-test.

9. (original) A built-in self-test controller including:

means for executing a memory built-in self-test; and

means for storing the results generated on execution of the memory executing means.

10. (original) The built-in self-test controller of claim 9, wherein the memory storing means includes the results of at least one paranoid check.

11. (original) The built-in self-test controller of claim 9, wherein the memory storing means includes a bit indicating whether the memory built-in self-test is done.

12. (currently amended) The built-in self-test controller of claim 9, wherein the memory executing means comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine ~~operating~~ configured to operate the memory built-in self-test state machine.

13. (currently amended) The built-in self-test controller of claim 9, wherein the memory executing means comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine ~~operating~~ configured to operate a predetermined one of the memory built-in self-test state machines.

14. (original) The built-in self-test controller of claim 9, further comprising:

means for executing a logic built-in self-test and storing the results thereof; and

means for storing the results of an executed logic built-in self-test.

15. (currently amended) An integrated circuit device including:

a plurality of memory components;

a testing interface; and

a built-in self-test controller controlled through the testing interface, the built-in self-test controller ~~including~~ comprising[[:]] a memory built-in self-test engine ~~capable of executing~~ configured to execute a memory built-in self-test[[;]] and to generate a memory

built-in self-test signature ~~generated~~ on execution of the memory built-in self-test wherein the built-in self-test signature comprises memory built-in self-test engine states.

16. (currently amended) The integrated circuit device of claim 15, wherein the memory built-in self-test signature ~~register is further capable of storing~~ comprises the results of at least one paranoid check.

17. (currently amended) The integrated circuit device of claim 15, wherein the memory built-in self-test signature ~~register~~ includes a bit indicating whether the memory built-in self-test is done.

18. (currently amended) The integrated circuit device of claim 15, wherein the memory built-in self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine ~~operating~~ configured to operate the memory built-in self-test state machine.

19. (currently amended) The integrated circuit device of claim 1~~5~~8, wherein the memory built-in self-test state machine ~~comprises~~ is configured to assume:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in ~~the~~ a memory built-in self-test domain in the initiate state;

a test state entered into from the flush state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

20. (currently amended) The integrated circuit device of claim 15, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine ~~operating~~ configured to operate a predetermined one of the memory built-in self-test state machines.

21. (original) The integrated circuit device of claim 15, wherein the memory components include a static random access memory device.

22. (original) The integrated circuit device of claim 15, wherein the testing interface comprises a Joint Test Action Group tap controller.

23. (currently amended) The integrated circuit device of claim 15, further comprising:

a logic built-in self-test engine ~~capable of executing~~ configured to execute a logic built-in self-test and storing the results thereof; and

a multiple input signature register ~~capable of storing~~ configured to store the results of an executed logic built-in self-test.

24. (currently amended) A method of performing a memory built-in self-test, the method comprising;

externally resetting a memory built-in self-test engine and a memory built-in self-test signature;

generating the memory built-in self-test signature upon an execution of a memory built-in self-test by the memory built-in self-test engine;

reading the generated memory built-in self-test signature wherein the built-in self-test signature comprises memory built-in self-test engine states.

25. (original) The method of claim 24, wherein the execution of the memory built-in self-test includes:

initiating a plurality of components and signals in a memory built-in self-test engine and the memory built-in self-test signature upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of components to a known state after initialization of the components and the signals; and

testing the flushed memory components.

26. (currently amended) The method of claim 2~~5~~4, wherein generating the memory built-in self-test signature includes[[:]] storing the results of the testing in a memory built-in a self-test signature register.

27. (original) The method of claim 24, wherein generating the memory built-in self-test signature includes storing the results of the testing in a memory built-in self-testing register.

28. (original) The method of claim 24, wherein performing the memory built-in self-test further includes at least one of:

performing at least one paranoid check; and

storing the results of the paranoid check in the memory built-in self-test signature register.

29. (original) The method of claim 24, wherein performing the memory built-in self-test includes setting a bit in the memory built-in self-test signature indicating whether the memory built-in self-test is done.

30. (original) The method of claim 24, wherein externally resetting the memory built-in self-test engine includes externally resetting the memory built-in self-test engine including:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine.

31. (original) The method of claim 30, wherein externally resetting the memory built-in self-test state machine includes externally resetting one of a plurality of memory built-in self-test state machines.

32. (currently amended) The method of claim ~~30~~ 25, wherein flushing ~~the~~ contents of the memory components includes flushing the contents of a plurality of static random access memories.

33. (currently amended) A method of performing a memory built-in self-test on an integrated circuit device, the method comprising;

interfacing the integrated circuit device with a tester;

performing a memory built-in self-test, including:

externally resetting a memory built-in self-test engine and a memory built-in self-test signature;

generating the memory built-in self-test signature upon an execution of a memory built-in self-test by the memory built-in self-test engine;

reading the generated memory built-in self-test signature wherein the built-in self-test signature comprises memory built-in self-test engine states.

34. (original) The method of claim 33, wherein the execution of the memory built-in self-test includes:

initiating a plurality of components and signals in a memory built-in self-test engine and the memory built-in self-test signature upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of components to a known state after initialization of the components and the signals; and

testing the flushed memory components.

35. (original) The method of claim 33, wherein generating the memory built-in self-test signature includes storing the results of the testing in a memory built-in self-test signature register.

36. (original) The method of claim 33, wherein performing the memory built-in self-test further includes at least one of:

performing at least one paranoid check; and

storing the results of the paranoid check in the memory built-in self-test signature register.

37. (original) The method of claim 33, wherein performing the memory built-in self-test further includes setting a bit in the memory built-in self-test signature indicating whether the memory built-in self-test is done.

38. (original) The method of claim 33, wherein externally resetting the memory built-in self-test engine includes externally resetting the memory built-in self-test engine including:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine.

39. (original) The method of claim 33, further comprising:

performing a logic built-in self-test; and

reading the results of the logic built-in self-test.